

What is claimed is:

1. A semiconductor device, comprising:  
chip interior areas formed on a wafer that are provided with functional elements, and scribe line areas formed on said wafer that serve as cutting space when dicing said wafer;  
5 a plurality of dummy patterns arranged in a diagonally forward skipped arrangement that are formed in said chip interior areas; and  
a plurality of dummy patterns arranged in grid form that are formed in said scribe line areas.
2. A semiconductor device according to claim 1, wherein:  
said semiconductor device includes a plurality of wiring layers that are stacked together, said dummy patterns being formed in said scribe line areas of each wiring layer; and  
5 said dummy patterns that are formed in said scribe line areas of each of said wiring layers are connected by via-holes.
3. A method of fabricating a semiconductor device that includes chip interior areas formed on a wafer that are provided with functional elements, and scribe line areas formed on said wafer that serve as cutting space when dicing said wafer; said method comprising:  
5 a step of both forming a plurality of dummy patterns in a diagonally forward skipped arrangement in said chip interior areas and forming a plurality of dummy patterns in a grid arrangement in said scribe line areas.

4. A method of fabricating a semiconductor device according to claim 3, wherein each of said dummy patterns that are formed in said scribe line areas has a square shape or a rectangular shape.

5. A method of fabricating a semiconductor device according to claim 3, wherein each of said dummy patterns that are formed in said chip interior areas has a square shape.

6. A method of fabricating a semiconductor device that includes chip interior areas formed on a wafer that are provided with functional elements, and scribe line areas formed on said wafer that serve as cutting space when dicing said wafer, and that further has a plurality of wiring layers that are stacked  
5 together, said method comprising;

a step of forming a plurality of dummy patterns in a diagonally forward skipped arrangement in said chip interior areas of each of said wiring layers and forming a plurality of dummy patterns in a grid arrangement in said scribe line areas of each of said wiring layers.

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7. A method of fabricating a semiconductor device according to claim 6, wherein each of said dummy patterns that are formed in said scribe line areas of each of said wiring layers has a square shape or a rectangular shape.

8. A method of fabricating a semiconductor device according to claim 6, wherein each of said dummy patterns that are formed in said chip interior areas of each of said wiring layers has a square shape.

9. A method of fabricating a semiconductor device according to claim 6, further comprising:

a step of connecting together said dummy patterns that are formed in said scribe line areas of each of said wiring layers by via-holes.

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